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Claims

[c1] A bipolar transistor, comprising:
a collector region;
an intrinsic base layer overlying said collector region, said intrinsic base layer including a single-crystal semiconductor;
an emitter disposed within a first opening overlying said intrinsic base layer;
a raised extrinsic base, including:
a raised extrinsic base layer overlying said intrinsic base layer; and
a link-up region electrically connecting said raised extrinsic base layer to said intrinsic base layer, said link-up region self-aligning said raised extrinsic base to said emitter, said link-up region disposed in a second opening separate from said first opening and in an undercut region extending from said second opening below said raised extrinsic base layer.

[c2] A bipolar transistor as claimed in claim 1, wherein said second opening is oriented in a vertical direction substantially perpendicular to said intrinsic base layer and said undercut region extends horizontally outward from

said second opening in a first direction towards said emitter.

[c3] A bipolar transistor as claimed in claim 2, wherein said second opening surrounds said emitter and has annular shape, wherein said undercut region further extends horizontally outward from said second opening in a second direction away from said emitter.

[c4] A bipolar transistor as claimed in claim 1, wherein said raised extrinsic base layer includes an inner portion disposed adjacent to said emitter and an outer portion opposite said second opening from said inner portion, wherein said link-up region electrically connects said inner portion to said outer portion.

[c5] A bipolar transistor as claimed in claim 4, further comprising a dielectric spacer disposed on a sidewall of said inner portion of said raised extrinsic base layer and of said link-up region, such that said inner portion and said link-up region are spaced from said emitter by a width of said spacer.

[c6] A bipolar transistor as claimed in claim 5, wherein said dielectric spacer includes an oxide spacer contacting a sidewall of said raised extrinsic base layer and a nitride spacer overlying said oxide spacer, said emitter contact-

ing a sidewall of said oxide spacer.

[c7] A bipolar transistor as claimed in claim 1, wherein said link-up region includes at least one material selected from the group consisting of doped semiconductors, metals and metal silicides.

[c8] A bipolar transistor as claimed in claim 1 wherein said raised extrinsic base layer includes a layer of a polycrystalline semiconductor and a low resistance layer overlying said polycrystalline semiconductor layer, said low resistance layer including at least one material selected from metals and metal silicides.

[c9] A heterojunction bipolar transistor (HBT) having a structure as claimed in claim 1, wherein said single-crystal semiconductor includes a semiconductor alloy, such that said intrinsic base layer forms a heterojunction with at least said collector region.

[c10] An HBT as claimed in claim 9, wherein said semiconductor alloy consists essentially of silicon germanium.

[c11] A method of making a bipolar transistor, comprising:
forming a structure including an intrinsic base overlying a collector region, said intrinsic base layer consisting essentially of a single-crystal semiconductor;
forming a dielectric layer over said intrinsic base layer

and a raised extrinsic base layer over said dielectric layer;

forming a sacrificial region in a first opening in said raised extrinsic base layer and said dielectric layer;

forming a second opening in said raised extrinsic base layer, said second opening separate from said first opening;

etching said dielectric layer from within said second opening to form an undercut region underlying said raised extrinsic base layer;

forming a link-up region in said second opening and said undercut region, said link-up region electrically connecting said raised extrinsic base layer to said intrinsic base layer;

removing said sacrificial region from said first opening; and

forming an emitter in said first opening, such that said link-up region and said raised extrinsic base layer are self-aligned to said emitter.

[c12] A method as claimed in claim 11 wherein said dielectric layer is formed to extend over said entire intrinsic base layer, and said first opening is formed by vertically etching said raised extrinsic base layer selective to a material of said dielectric layer, and thereafter removing said dielectric layer from within said first opening.

[c13] A method as claimed in claim 11, wherein said dielectric layer is etched to form said undercut region by etching selectively to a material of said sacrificial region.

[c14] A method as claimed in claim 13 wherein said dielectric layer consists essentially of an oxide and said material of said sacrificial region consists essentially of a nitride.

[c15] A method as claimed in claim 11, wherein said second opening is formed in a vertically oriented direction substantially perpendicular to said intrinsic base layer and said undercut region is formed to extend horizontally outward from said second opening in a first direction towards said sacrificial region.

[c16] A method as claimed in claim 15, wherein said second opening surrounds said sacrificial region and has annular shape, wherein said undercut region is further formed to extend horizontally outward from said second opening in a second direction away from said sacrificial region.

[c17] A method as claimed in claim 11, wherein said link-up region includes at least one material selected from the group consisting of doped semiconductors, metals and metal silicides.

[c18] A method as claimed in claim 11 wherein said step of forming said emitter includes removing said sacrificial region from said first opening to expose sidewalls of said link-up layer and said raised extrinsic base layer, forming at least one dielectric spacer on said exposed sidewalls, and thereafter filling said first opening with a material selected from doped semiconductors, metals and metal silicides.

[c19] A method as claimed in claim 18 wherein said at least one dielectric spacer includes a first spacer contacting said exposed sidewalls and having an L-shape, said first spacer consisting essentially of an oxide, and a second spacer consisting essentially of a nitride disposed over said first spacer.

[c20] A method as claimed in claim 11 wherein said second opening is disposed surrounding said sacrificial region.

[c21] A method as claimed in claim 20 wherein said second opening has an annular shape.

[c22] A method as claimed in claim 11 wherein said raised extrinsic base layer includes a layer of a polycrystalline semiconductor material and a low-resistance layer overlying said polycrystalline semiconductor layer, said low resistance layer including at least one material selected

from metals and metal silicides.

[c23] A method as claimed in claim 11, wherein said single-crystal semiconductor includes a semiconductor alloy, such that said intrinsic base layer forms a heterojunction with at least said collector region.